EAST - [2536a.wsp:1]

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- L19: (0) 15 AND POLYGATE
- L20: (5) "6362049"
- L21: (6977) (peripher$4 active memory near3 (region area)) with ('sti' shallow adj trench isolato...
- L22: (4043) 21 and polysilicon
- L23: (1458) 21 and (polysilicon with mask$4)
- L24: (47342) "24" and (remov$3 with mask$3)
- L25: (1039) 23 and (remov$3 with mask$3)
- L28: (5) 26 and (mask$3 with dish$3)
- L26: (945) 25 and (peripher$4 active near3 (region area)) with ('sti' shallow adj trench isolator...
- L29: (414) (peripher$4 near3 (region area)) with ('sti' shallow adj trench isolator 'locos' 'fox')
- L30: (126) 29 and floating
- L31: (89) 30 and (polysilicon near3 layer)
- L32: (75) 31 and (polysilicon with etch$3)
- L33: (62) 32 and (mask$4 with etch$3)
- L34: (42) 33 and polysilicon with mask
- L35: (1) 34 and dish$3
- L36: (1035) (polysilicon with mask$3) with ((peripher$3 active core) near3 (region area))
- L37: (32) (polysilicon with mask$3) with (((peripher$3 active core) near3 (region area)) with ('s...
- L38: (219) ((polysilicon nitride) with mask$3) with (((peripher$3 active core) near3 (region area...
- L39: (31) ((polysilicon nitride) with protect$3) with (((peripher$3 active core) near3 (region ar...
- L40: (10) 38 and ('cmp' (chemical adj mechanical adj posh$3)) with polysilicon
- L41: (105) ((peripher$3 meory active) near3 (region area)) with ((self adj aligned) near3 (float...
- L42: (81) 41 and ('sti' isolator 'fox' 'locos')
- L43: (81) 42 and (dielectric insulat$3)
- L44: (51) 43 and (polysilicon (silicon adj nitride)) with ((protect$3 mask$4) near4 layer)
- L45: (51) 44 and ('cmp' remov$3 polish$3 planar$6) with (polysilicon silicon adj nitride (protec

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44 and ('cmp' remov$3 polish$3 planar$6) with (poly silicon silicon adj nitride (protect$3 mask$4) near4 layer)

BRS form | S&R form | Image | Text

	U	1	Document ID	Issue Date	Pages	Title	Current OR	Current XR	Retrieval C	Inventor	S	C	P	2	3		
22	☐	☐	US 6756631 B2	20040629	18	Stacked-gate cell structure and its NAND-type flash memory array	257/316	257/317; 257/319; 257/320;		Wu; Ching-Yuan	☑	☐	☐	☐	☐	☐	☐

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EAST - [25\3a.wap:1]

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1 L45: (51) 44 and ('cmp' remov$3 polish$3 planar$6) with (polysilicon silicon adj nitride (protec...

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OPS form | ISR form | Image | Text

	U	1	Document ID	Issue Date	Pages	Title	Current OR	Current XR	Retrieval	Inventor	S	C	P	2	3	4	5
1			US 20040185637	20040923	11	METHOD TO PRESERVE ALIGNMENT MARK OPTIC	438/401			Fu, Shih-Chi et al.							
2			US 20040173869	20040909	12	Process for self-aligned manufacture of integrated elec	257/510	257/E21.548; 257/E21.549;		Bez, Roberto et al.							
3			US 20040166643	20040826	10	Semiconductor isolator system	438/296	257/E21.209; 257/E21.422		Doan, Trung Tri et al.							
4			US 20040166633	20040826	15	Method of fabricating cell of nonvolatile memory device w	438/261	257/E21.682; 257/E27.103;		Lee, Chang-Hyun et al.							
5			US 20040094795	20040520	13	SELF-ALIGNED FLOATING-GATE STRUCT	257/316	257/E29.129		Wu, Ching-Yuan							
6			US 20040094794	20040520	21	STACKED-GATE CELL STRUCTURE AND ITS NAN	257/316	257/E21.682; 257/E21.69;		Wu, Ching-Yuan							
7			US 20030199149	20031023	17	Shallow trench isolation method and method for manu	438/424	257/E21.546; 257/E21.682;		Lee, Seong-Soo et al.							
8			US 20030151084	20030814	16	Cells of nonvolatile memory devices with floating gates an	257/315	257/E21.682; 257/E27.103		Lee, Chang-Hyun et al.							
9			US 20030143808	20030731	12	FABRICATION METHOD FOR FLASH MEMORY	438/257	257/E21.682; 257/E27.103;		Jang, Wen-Yueh							
10			US 20030143790	20030731	25	Methods of fabricating a stack-gate flash memory array	438/197			Wu, Ching-Yuan							
11			US 20030141535	20030731	12	FABRICATION METHOD FOR FLASH MEMORY	257/314	257/321; 257/E21.682;		Jang, Wen-Yueh							
12			US 20030073291	20030417	7	Method of forming stacked gate for flash memories	438/296	257/E21.546; 257/E21.682;		Tseng, Horng-Huei							
13			US 20020142544	20021003	8	Method of forming a self-aligned floating gate poly	438/257	257/315; 257/332;		Wang, Chih Hsin							
14			US 20020102793	20020801	20	Method of fabricating a scalable stacked-gate flash me	438/257	257/E21.689; 257/E27.081;		Wu, Ching-Yuan							
15			US 20020072197	20020613	28	Method for self-aligned shallow trench isolation and	438/424	257/E21.549; 257/E21.628		Kang, Man-Sug et al.							
16			US 20020027241	20020307	16	Novel split-gate flash cell	257/314	257/324		Sung, Hung-Cheng et al.							

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1.45 (51) 44 and ('cmp' remov$3 polish$3 planar$6) with (polysilicon silicon adj nitride (protec...

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	U	1	Document ID	Issue Date	Pages	Title	Current OR	Current XR	Retrieval	Inventor	S	C	P	2	3	4	5
18	☐	☐	US 20010022375	20010920	13	Method to fabricate a new structure with multi-self-align	257/298	257/256; 257/314;		Hsieh, Chia-Ta et al.	☑	☐	☐	☐	☐	☐	☐
19	☐	☐	US 20010012662	20010809	16	A new structure to fabricate split-gate with self-aligned so	438/257	257/E21.209; 257/E21.682;		Hsieh, Chia-Ta et al.	☑	☐	☐	☐	☐	☐	☐
20	☐	☐	US 20010002714	20010607	12	Method for fabricating floating gate semiconductor d	257/316	257/510; 257/E21.209;		Doan, Trung Tri	☑	☐	☐	☐	☐	☐	☐
21	☐	☐	US 6803291 B1	20041012	10	Method to preserve alignment mark optical integrity	438/401	257/797		Fu; Shih-Chi et al.	☑	☐	☐	☐	☐	☐	☐
22	☐	☐	US 6756631 B2	20040629	18	Stacked-gate cell structure and its NAND-type flash mem	257/316	257/317; 257/319;		Wu; Ching-Yuan	☑	☐	☐	☐	☐	☐	☐
23	☐	☐	US 6743695 B2	20040601	17	Shallow trench isolation method and method for manu	438/439	257/374; 257/E21.546;		Lee; Seong-Soo et al.	☑	☐	☐	☐	☐	☐	☐
24	☐	☐	US 6720611 B2	20040413	12	Fabrication method for flash memory	257/315	257/316; 257/321;		Jang; Wen-Yueh	☑	☐	☐	☐	☐	☐	☐
25	☐	☐	US 6689658 B2	20040210	24	Methods of fabricating a stack-gate flash memory array	438/257	257/315; 257/321;		Wu; Ching-Yuan	☑	☐	☐	☐	☐	☐	☐
26	☐	☐	US 6686243 B2	20040203	12	Fabrication method for flash memory	438/259	257/316; 257/E21.682;		Jang; Wen-Yueh	☑	☐	☐	☐	☐	☐	☐
27	☐	☐	US 6677224 B2	20040113	7	Method of forming stacked gate for flash memories	438/593	257/E21.546; 257/E21.682;		Tseng; Horng-Huei	☑	☐	☐	☐	☐	☐	☐
28	☐	☐	US 6627942 B2	20030930	6	Self-aligned floating gate poly for a flash E2PROM cell	257/315	257/314; 257/317;		Wang; Chih Hsin	☑	☐	☐	☐	☐	☐	☐
29	☐	☐	US 6605506 B2	20030812	19	Method of fabricating a scalable stacked-gate flash me	438/257	257/E21.689; 257/E27.081;		Wu; Ching-Yuan	☑	☐	☐	☐	☐	☐	☐
30	☐	☐	US 6548374 B2	20030415	16	Method for self-aligned shallow trench isolation and	438/424	257/E21.546; 257/E21.628;		Chung; Byung-Hong	☑	☐	☐	☐	☐	☐	☐
31	☐	☐	US 6538277 B2	20030325	14	Split-gate flash cell	257/317	257/315; 257/321;		Sung; Hung-Cheng et al.	☑	☐	☐	☐	☐	☐	☐
32	☐	☐	US 6495853 B1	20021217	11	Self-aligned gate semiconductor	257/30	257/314; 257/315;		Holbrook; Allison et al.	☑	☐	☐	☐	☐	☐	☐
33	☑	☐	US 6479859 B2	20021112	13	Split gate flash memory with multiple self-alignments	257/315	257/314; 257/E21.682;		Hsieh; Chia-Ta et al.	☐	☐	☐	☐	☐	☐	☐

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L45: (51) 44 and ('cmp' remov$3 polish$3 planar$6) with (polysilicon silicon adj nitride (protec...

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	U	1	Document ID	Issue Date	Pages	Title	Current OR	Current XR	Retrieval	Inventor	S	C	P	2	3	4	5
34			US 6403494 B1	20020611	13	Method of forming a floating gate self-aligned to STI on EE	438/719	438/257; 438/735		Chu; Wen-Ting et al.							
35			US 6380035 B1	20020430	16	Poly tip formation and self-align source process for s	438/264	257/E21.682; 257/E29.129;		Sung; Hung-Cheng et al.							
36			US 6326263 B1	20011204	11	Method of fabricating a flash memory cell	438/257	257/316; 257/E21.682;		Hsieh; Tsong-Minn							
37			US 6316804 B1	20011113	9	Oxygen implant self-aligned, floating gate and isolation stru	257/315	257/316; 257/506;		Templeton; Michael K. et al.							
38			US 6309928 B1	20011030	15	Split-gate flash cell	438/265	438/257; 438/259;		Sung; Hung-Cheng et al.							
39			US 6281103 B1	20010828	13	Method for fabricating gate semiconductor	438/593	257/E21.209; 257/E21.422;		Doan; Trung Tri							
40			US 6271561 B1	20010807	11	Method for fabricating floating gate semiconductor d	257/316	257/510; 257/E21.209;		Doan; Trung Tri							
41			US 6259131 B1	20010710	15	Poly tip and self aligned source for split-gate flash cell	257/315	257/321; 257/322;		Sung; Hung-Cheng et al.							
42			US 6228713 B1	20010508	14	Self-aligned floating gate for memory application using sha	438/257	257/314; 257/315;		Pradeep; Yelehanka Ramachandramurthy et							
43			US 6228695 B1	20010508	15	Method to fabricate split-gate with self-aligned source and s	438/201	257/E21.209; 257/E21.682;		Hsieh; Chia-Ta et al.							
44			US 6221715 B1	20010424	11	Method of making polysilicon self-aligned to field isolation	438/257	257/E21.422; 257/E21.682;		Chen; Bin-Shing							
45			US 6204126 B1	20010320	13	Method to fabricate a new structure with multi-self-align	438/267	257/E21.682; 257/E27.103;		Hsieh; Chia-Ta et al.							
46			US 6200856 B1	20010313	10	Method of fabricating self-aligned stacked gate flash	438/257	257/E21.682		Chen; Bin-Shing							
47			US 6172395 B1	20010109	14	Method of manufacture of self-aligned floating gate, flas	257/315	257/346; 257/401;		Chen; Jong et al.							
48			US 6171908 B1	20010109	11	Method of fabricating self-aligned split gate flash me	438/266	257/E21.422; 257/E29.129;		Chen; Bin-Shing							
49			US 6117733 A	20000912	18	Poly tip formation and self-align source process for s	438/265	257/288; 257/314;		Sung; Hung-Cheng et al.							

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